Source-Side High-*k* Dual-Material Asymmetric Gate MOSFETs: Stepped-Potential Modulation and TCAD Optimization of Subthreshold Leakage at 40nm Node

Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan.
Department of Materials Science and Engineering, National Cheng Kung University, Tainan 701, Taiwan.
Student: Chun-Wei Chang (張竣爲) Advisor: Prof. Meng-Hsueh Chiang (江孟學 教授)

Abstract

This study performs TCAD electrostatic physical simulations and structural optimizations to resolve severe short-channel effects (SCE) and switching current ratio encountered when scaling channel length down to $L_g = 40$ nm. First, an optimal baseline device (n422) strictly meeting the target switching current ratio $\log_{10}(I_{ON}/I_{OFF}) \geq 7.0$ was extracted from 9 parameter split nodes at 120 nm. For the extreme 40 nm node, an innovative **Source-Side High-*k* Dual-Material Asymmetric Gate** structure (where the source-side dielectric thickness is about 3 times that of the drain side) is introduced to investigate its "Stepped-Potential Modulation" mechanism within the channel. Results demonstrate that under the golden length ratio $L_1/L_g = 0.67$, Drain-Induced Barrier Lowering (DIBL) is dramatically suppressed from 568.00 mV/V to 61.38 mV/V, subthreshold leakage I_{OFF} drops by over 5 orders of magnitude (148.5 μA → 0.667 nA), and the current ratio recovers to 6.59 Decades, successfully resolving the electrostatic breakdown in deep sub-micron MOSFETs.

TCAD Simulation Workflow

1. Baseline Screening
9 Split Nodes
Screening

→

2. Scaling SCE Analysis
Lg = 40nm SCE
Breakdown

→

3. Structural Innovation
Source-Side High-*k* DMG

→

4. Performance Comparison
of Improved & Original

Results & Discussion

120nm Baseline Screening

I_{ON} : Measured I_D at $V_{GS} = V_{DS} = V_{DD} = 1.5$ V
I_{OFF} : Measured I_D at $V_{GS} = 0$ V, $V_{DS} = V_{DD}$

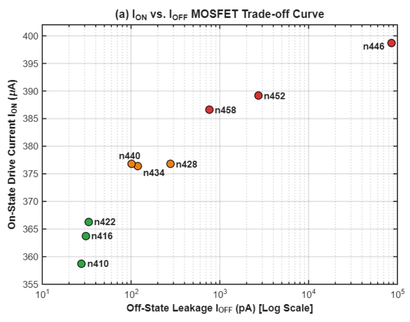

Fig. 1 I_{ON} vs. I_{OFF} MOSFET trade-off curve across 9 split nodes

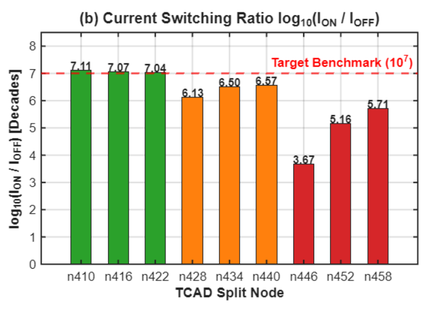

Fig. 2 Switching current ratio benchmark (n422 meets target > 10^7)

Short-Channel Effect Characterization

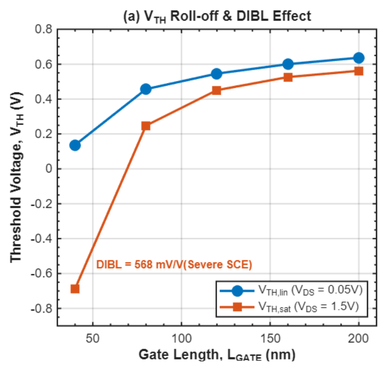

Fig. 3 V_{TH} roll-off and severe DIBL (568 mV/V) at $L_g = 40$ nm.

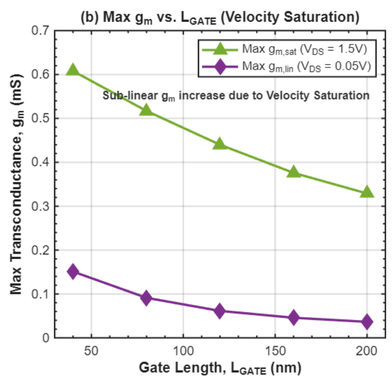

Fig. 4 Max g_m vs. L_{GATE} under velocity saturation.

Source-Side High-k DMG Optimization & Results

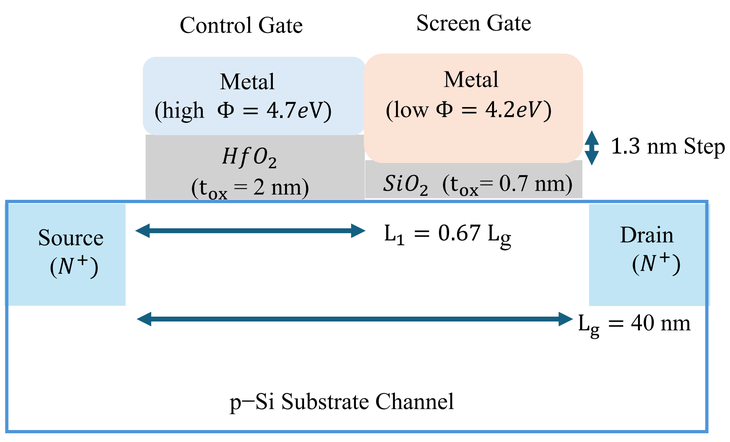

Fig. 5 **Source-Side High-k DMG Structure** ($L_1/L_g = 0.67$) (Note: Conventional baseline uses single 4.2 eV gate with uniform 0.7 nm SiO_2)

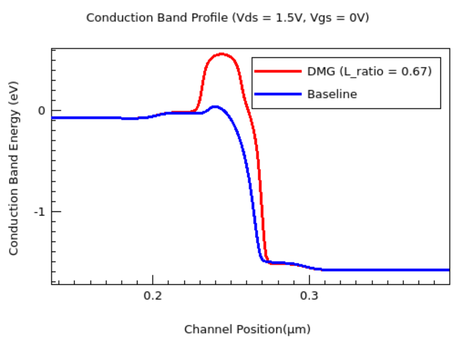

Fig. 6 Off-state conduction band profile (stepped-potential modulation)

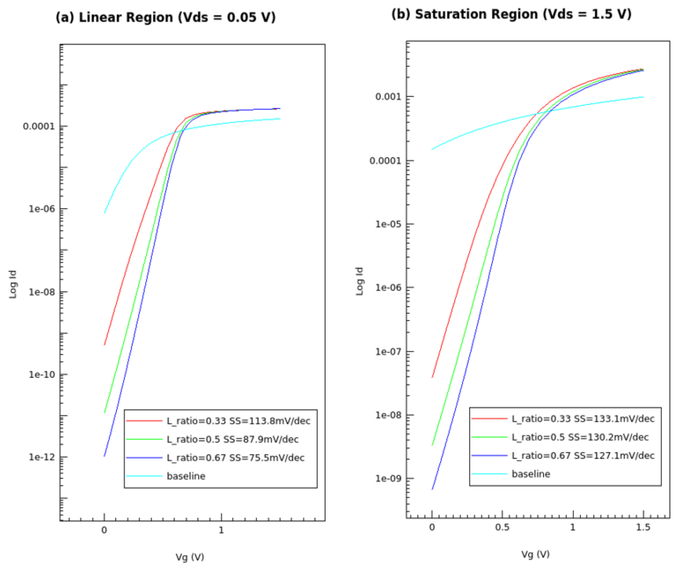

Fig. 7 $I_d - V_g$ transfer characteristics in linear (0.05 V) and saturation (1.5 V) regions.

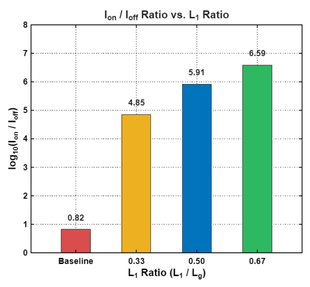

Fig. 8 Current ratio reaches 6.59 decades ($L_1/L_g = 0.67$)

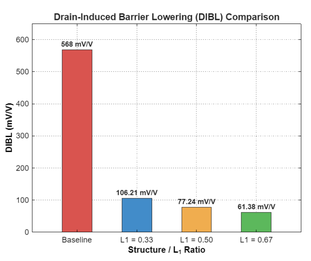

Fig. 9 DIBL comparison (suppressed by 89.2% down to 61.38 mV/V)

Conclusions

1. Baseline Calibration at 120 nm: TCAD simulation calibrates the 120-nm baseline device (n422), exhibiting optimal electrostatic control with DIBL = 65.52 mV/V and SS ≈ 82 mV/dec, satisfying the high-performance logic switching requirement ($I_{ON}/I_{OFF} > 10^7$).
2. Scaling Crisis in Conventional 40-nm Devices: Aggressive scaling down to 40 nm induces severe Short-Channel Effects (SCEs) in conventional single-material structures. The intense drain field causes catastrophic barrier degradation (DIBL = 568.00 mV/V) and a subthreshold leakage explosion (I_{OFF} = 148.5 μA), leading to the breakdown of digital switching functionality.
3. Conduction Band Profile Modulation & Performance Breakthrough: Extraction of the off-state conduction band profile (E_c) demonstrates the physical efficacy of the proposed Source-Side High-*k* Dual-Material Asymmetric Gate ($L_1/L_g = 0.67$, 3:1 oxide thickness ratio). The high-work-function Control Gate effectively elevates the source-side energy barrier, while the Screen Gate shields against drain field penetration. Consequently, DIBL is reduced by 89.2% (down to 61.38 mV/V) and off-state leakage is suppressed by over 5 orders of magnitude (down to 0.667 nA), validating its ultra-low-power capability for nanoscale CMOS technology.