

Investigation of Orientation-Dependent Performance and Self-Heating Effects in TreeFET and NSFET for N/P Matching Enhancement



國立成功大學
National Cheng Kung University

Min-Chieh Huang, Wei-Chen Tu

Department of Electrical Engineering, National Cheng Kung University

E-mail: wctu@gs.ncku.edu.tw

Abstract

This study compares TreeFET (2/3 sheets) and NSFET (3/4 sheets) architectures via Sentaurus TCAD. TreeFET's vertical sidewalls leverage orientation-dependent mobility for superior N/P matching. Self-Heating Effect (SHE) analysis reveals that TreeFET's vertical heat dissipation path effectively reduces T_{MAX} and I_{ON} degradation. These findings provide a good solution for advanced GAA scaling.

Device Structure

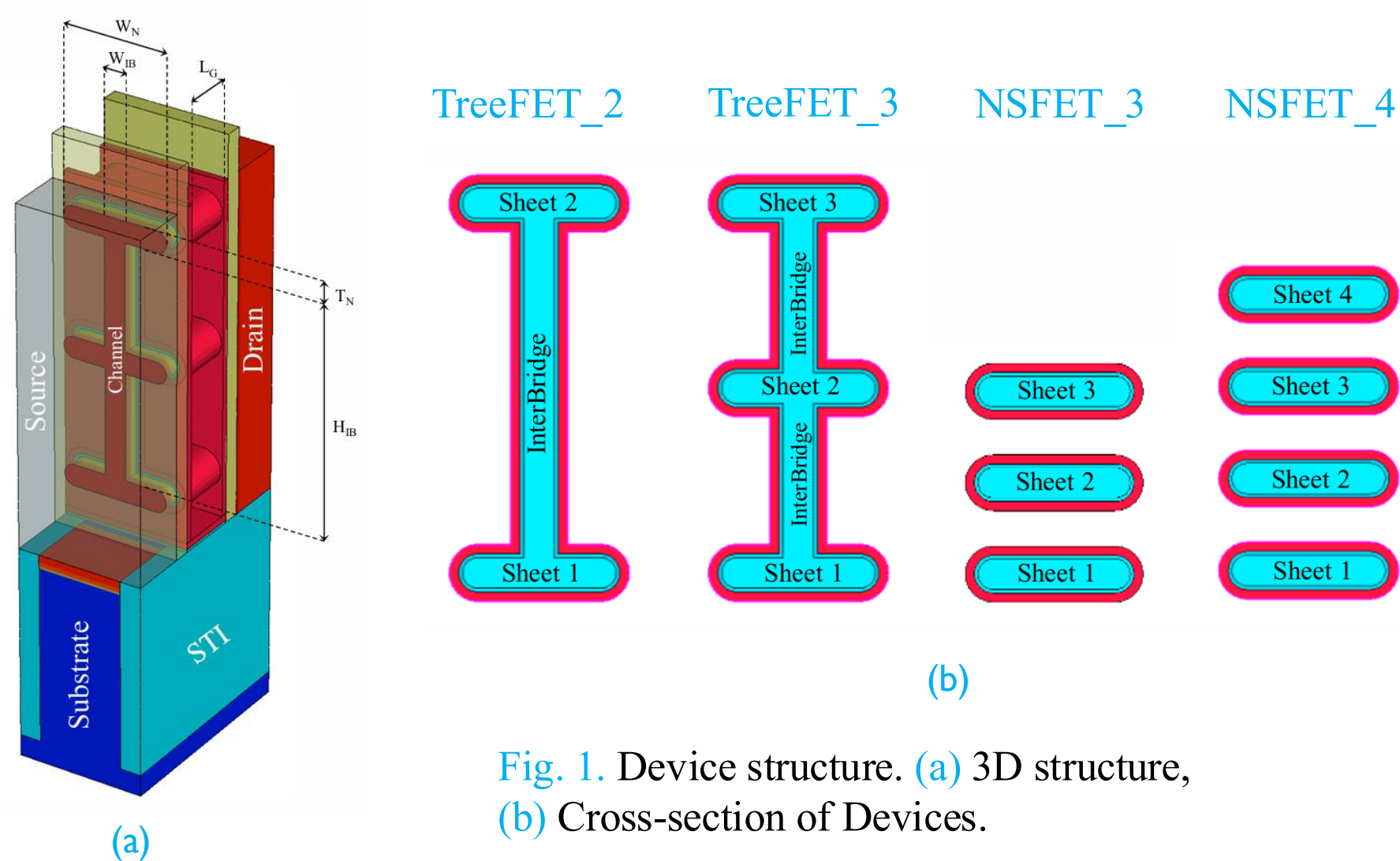


Fig. 1. Device structure. (a) 3D structure, (b) Cross-section of Devices.

Device and Thermal Specifications

Device Parameter	TreeFET_2	TreeFET_3	NSFET_3	NSFET_4
Gate Length (L_G)	12 nm	12 nm	12 nm	12 nm
Number of Nanosheets	2	3	3	4
Nanosheet Thickness (T_N)	5 nm	5 nm	5 nm	5 nm
Nanosheet Width (W_N)	30nm	30nm	30nm	30nm
Height of Interbridge (H_{IB})	55nm	55nm	-	-
Width of Interbridge (W_{IB})	5nm	5nm	-	-
Effective Width (W_{eff})	180 nm	260 nm	180 nm	260 nm
Source/Drain Doping	$1 \times 10^{20} \text{ cm}^{-3}$	$1 \times 10^{20} \text{ cm}^{-3}$	$1 \times 10^{20} \text{ cm}^{-3}$	$1 \times 10^{20} \text{ cm}^{-3}$
Channel Doping	$1 \times 10^{16} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$
Substrate Doping	$5 \times 10^{18} \text{ cm}^{-3}$	$5 \times 10^{18} \text{ cm}^{-3}$	$5 \times 10^{18} \text{ cm}^{-3}$	$5 \times 10^{18} \text{ cm}^{-3}$
Work Function (N/PMOS)	4.43/4.83 eV	4.43/4.83 eV	4.43/4.83 eV	4.43/4.83 eV

Symbol	Quantity	Value
$R_{Electrode}$	Electrode Surface Resistance	$1 \times 10^{-5} \text{ m}^2 \text{ K/W}$
κ_{Ch}	Channel Thermal Conductivity	14.45 W/K.m
$\kappa_{S/D}$	S/D Thermal Conductivity	38 W/K.m
κ_{OX}	Oxide Thermal Conductivity	2.5 W/K.m
κ_{Cnt}	Contact Thermal Conductivity	200 W/K.m
κ_{Sp}	Spacer Thermal Conductivity	2 W/K.m
κ_{Sub}	Sub. Thermal Conductivity	140 W/K.m
κ_{Metal}	Gate Metal Thermal Conductivity	238 W/K.m

(b)

Fig. 2. Device and Thermal Specifications: (a) Device Parameter, (b) Thermal Specifications.

Orientation Analysis

Fig. 3(a)(b) show the NMOS/PMOS transfer characteristics, where TreeFET shows higher PMOS current due to its (110) sidewall hole-mobility advantage. Fig. 3(c) compares the matching ratio, defined as

$$\text{Matching Ratio} = \frac{|I_{ON, P}|}{I_{ON, N}}$$

where a value closer to 1 indicates better N/P matching. TreeFET_2 shows the best matching, TreeFET_3 is slightly worse because of its similarity to NSFET, and NSFET_3 shows the worst matching performance. Fig. 3(d) compares the DIBL values, showing that the matching improvement is achieved while maintaining acceptable short-channel control.

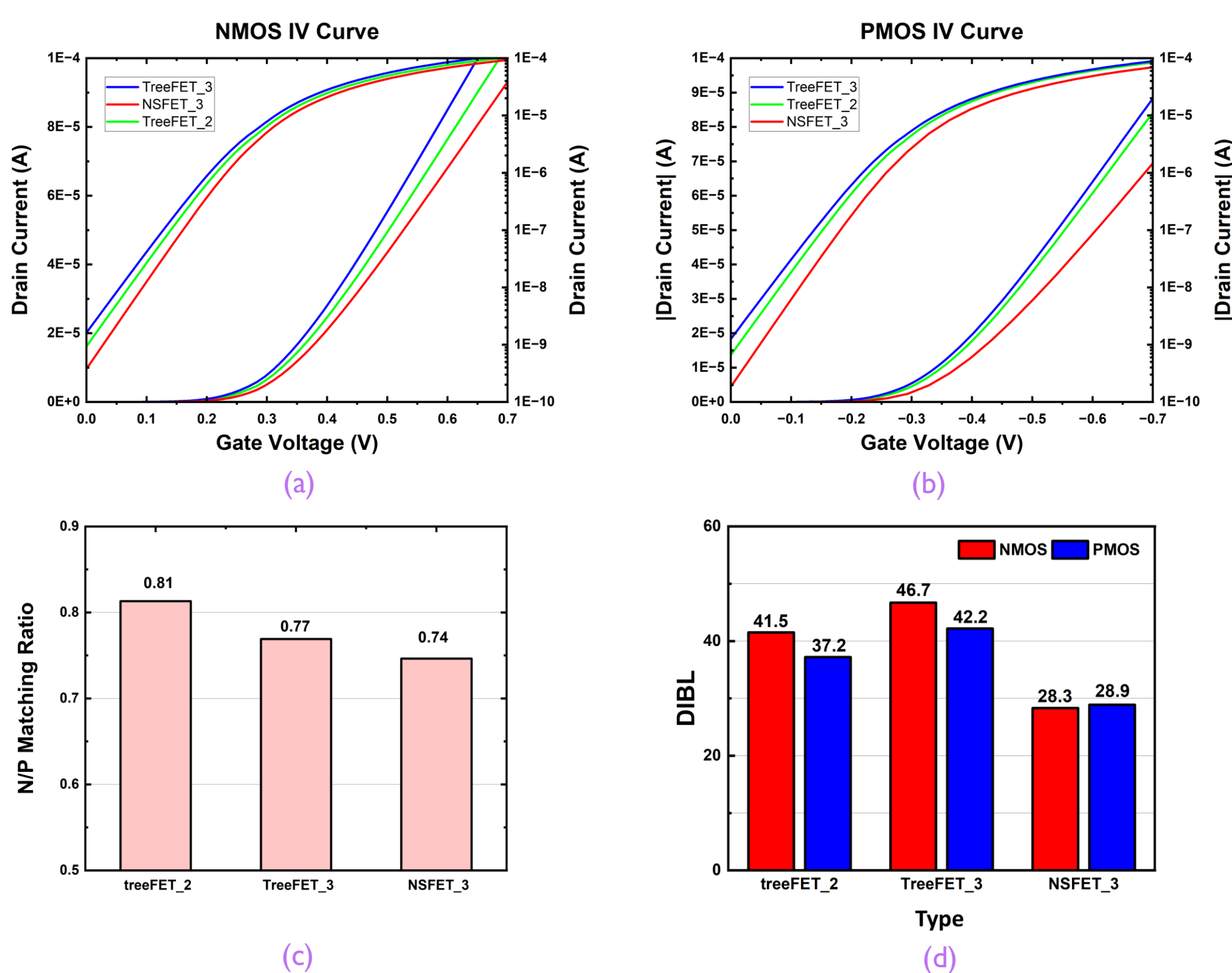


Fig. 3. Orientation analysis of TreeFET and NSFET devices: (a) NMOS transfer characteristics, (b) PMOS transfer characteristics, (c) Comparison of N/P matching ratio, (d) DIBL comparison.

Self-Heating Effect (S.H.E.) Analysis

TreeFET improves heat dissipation via its vertical interbridge structure. As shown in Fig. 4(a)(b), TreeFET_3 maintains a lower T_{MAX} (393.0 K) than NSFET_4 (400.1 K) at the same W_{eff} .

According to Fig. 4(c)(d), TreeFET_3 exhibits less I_{ON} degradation than NSFET_4, while fewer channels (TreeFET_2 vs. TreeFET_3) further lessen heat accumulation. This confirms that the TreeFET design effectively suppresses self-heating effects.

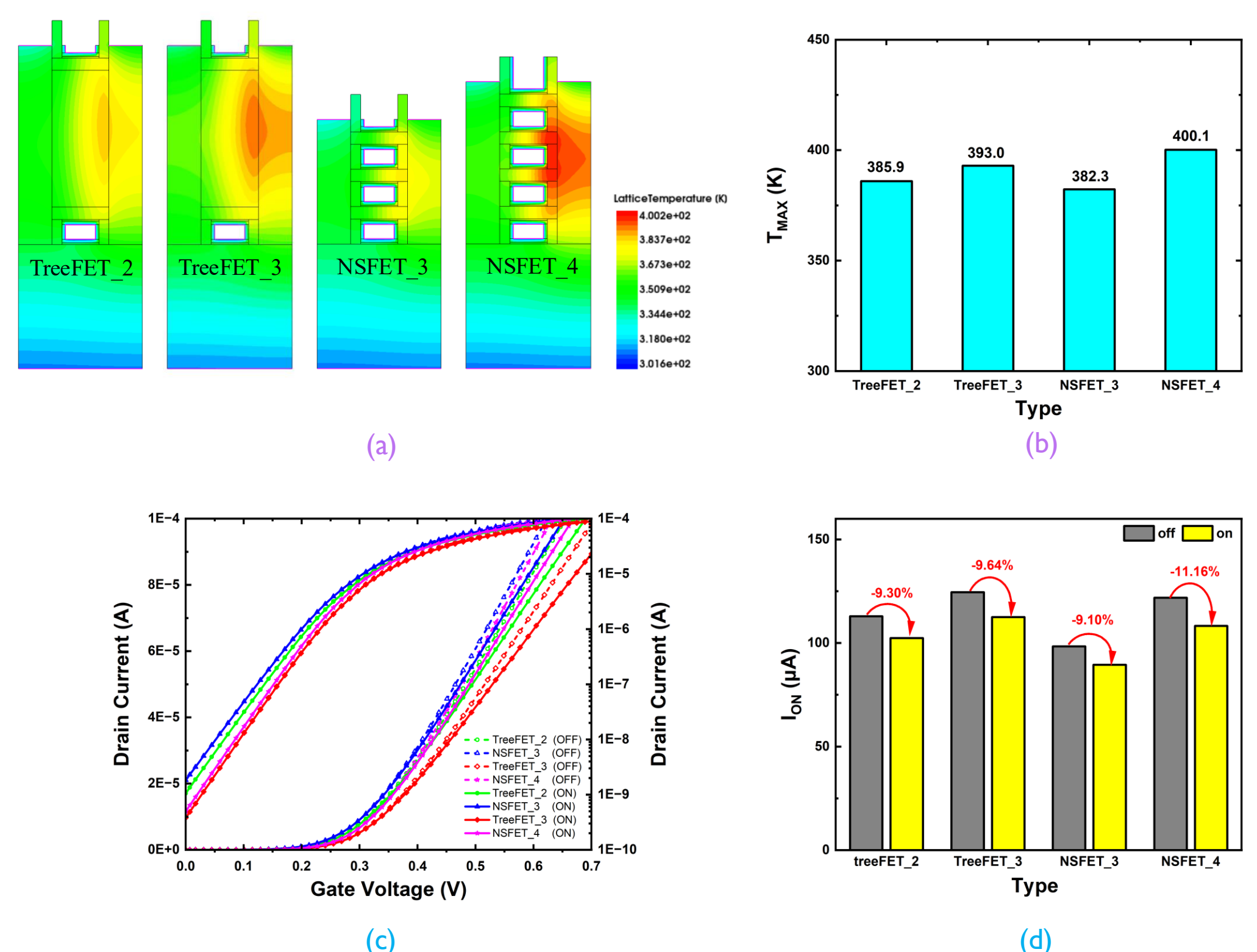


Fig. 4. SHE analysis of TreeFET and NSFET devices: (a) Lattice temperature distribution, (b) Comparison of maximum lattice temperature (T_{MAX}), (c) Transfer characteristics with and without SHE, (d) Impact of SHE on drain current (I_{ON}).

Conclusion

This study shows that TreeFET improves PMOS drive current through its vertical sidewall orientation, resulting in a better N/P matching ratio compared with NSFET. In addition, vertical interbridge structure provides an effective heat dissipation path, leading to lower maximum lattice temperature and smaller I_{ON} degradation. Therefore, TreeFET shows strong potential for advanced GAA transistor design with improved N/P matching and suppressed self-heating effects.