

Investigation of DC Performance Enhancement and AC RC Delay Trade-offs in Forksheet FETs via Outer Wall Engineering



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Abstract

This study investigates DC performance enhancements and AC RC delay trade-offs in Forksheet FETs via outer wall engineering. Deeper etching improves electrostatic control, maintaining stable V_{th} and VTC while minimizing DIBL. This steepens subthreshold swing, accelerating turn-off and drastically reducing short-circuit power. Conversely, it exacerbates fringing fields, increasing parasitic capacitance (C_{gg}) and prolonging RC delay. Optimizing this structural trade-off is vital for next-generation logic circuits.

Device Structure

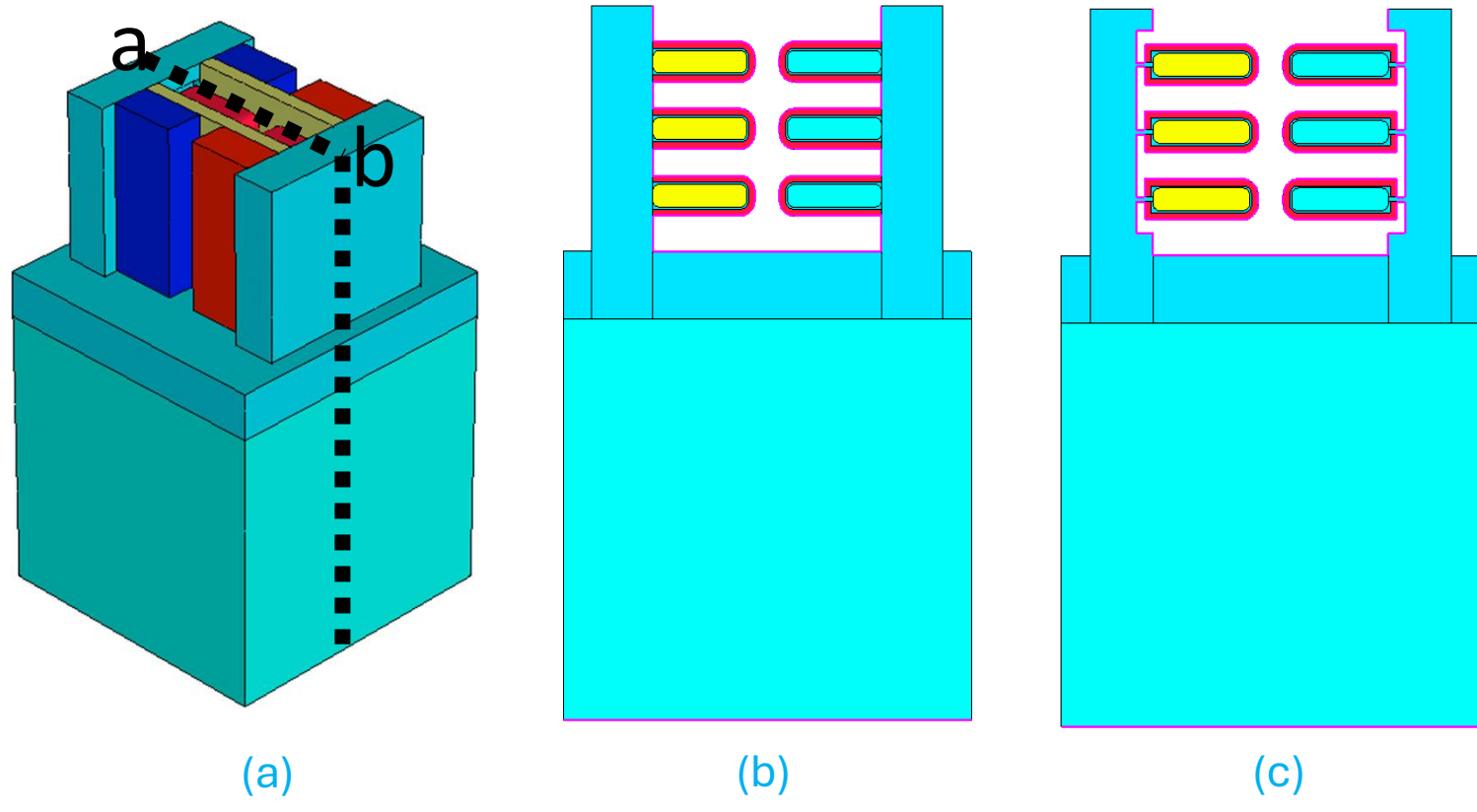


Fig. 1. Device structure. (a) 3D structure, (b) Outer wall Forksheet without etching, (c) Outer wall Forksheet with etch depth 5nm

Process Flow

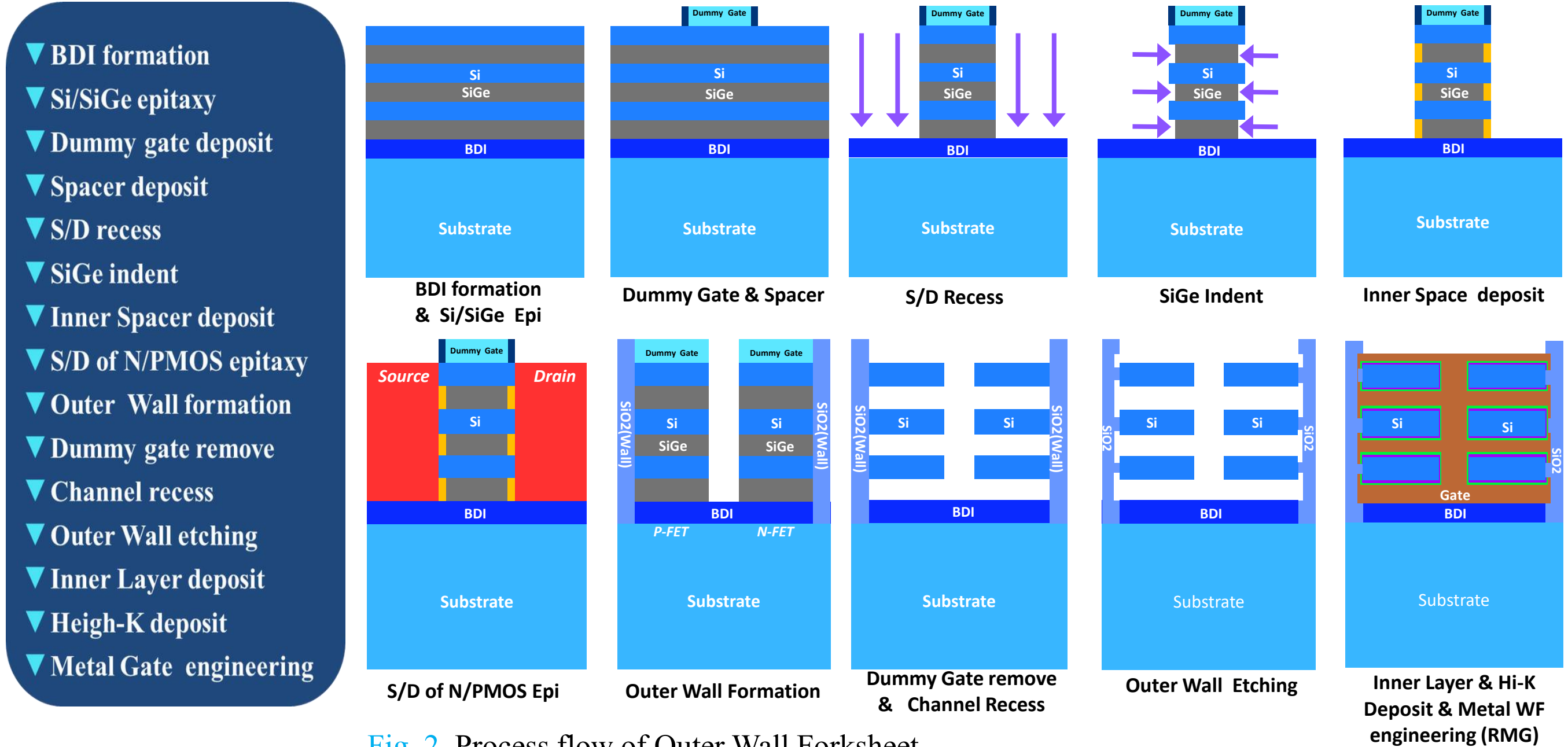


Fig. 2. Process flow of Outer Wall Forksheet.

Simulation Result

Threshold voltages (V_{th}) exhibit robust stability across varying etch depths. This keeps the Voltage Transfer Characteristics (VTC) completely unshifted. Governed by $V_M = \frac{V_{DD} - |V_{th,p}| + k_R V_{th,n}}{1 + k_R}$, the constant V_{th} fixes the switching threshold (V_M), ensuring an optimal logic noise margin. Furthermore, outer wall engineering strongly suppresses short-channel effects, significantly minimizing DIBL.

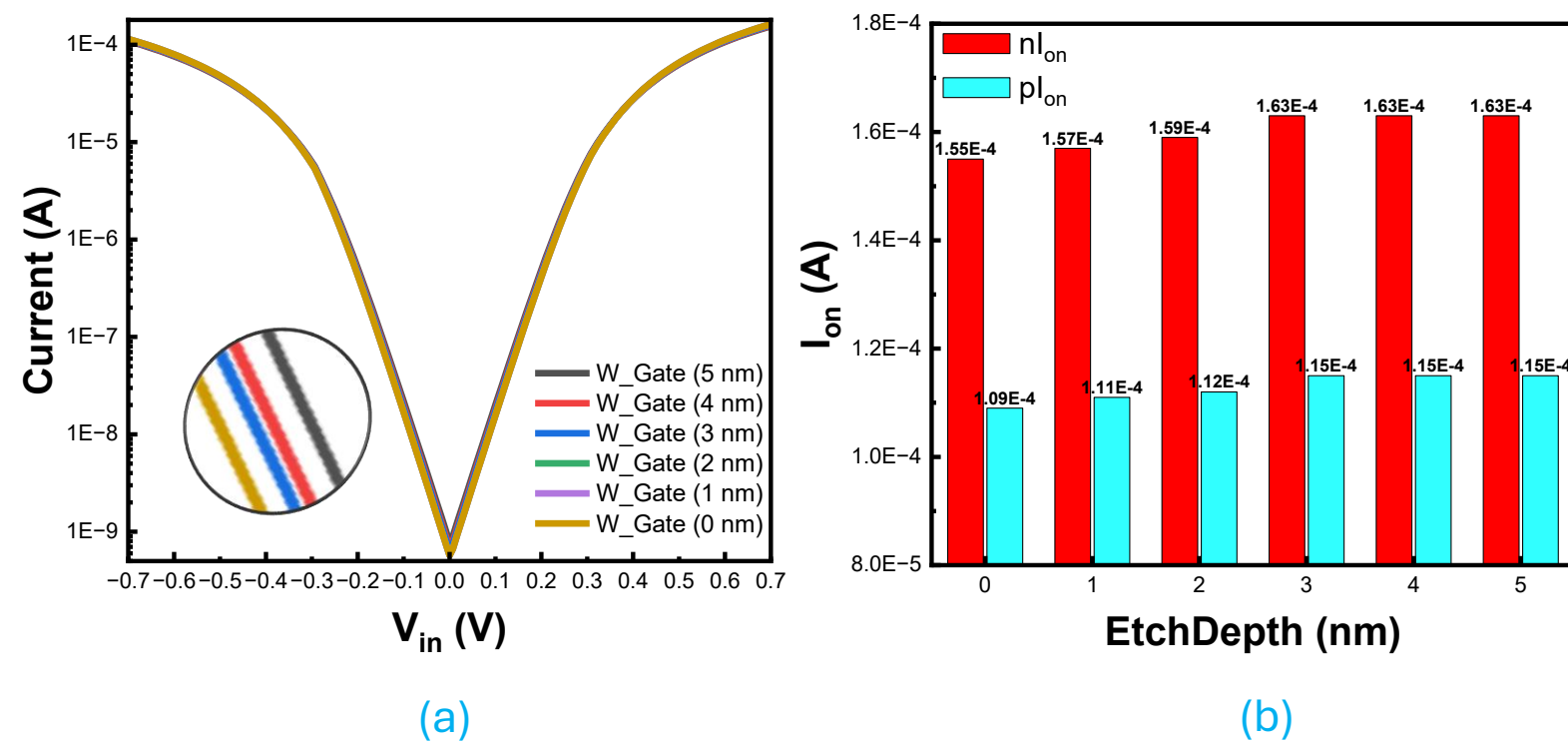


Fig. 3. (a) $I_d V_g$ curve, (b) I_{on} of N-type and P-type

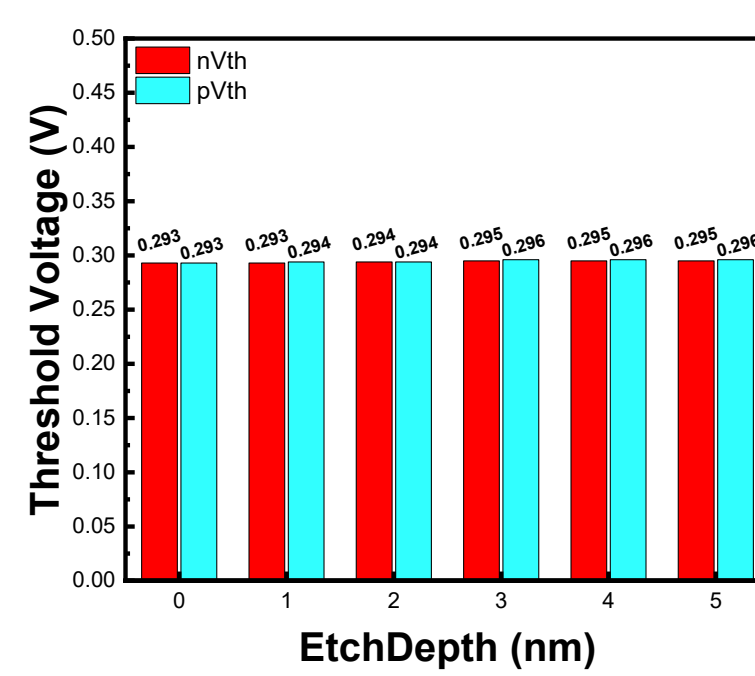


Fig. 4. V_{th} of Outer Wall Forksheet in different etch depths

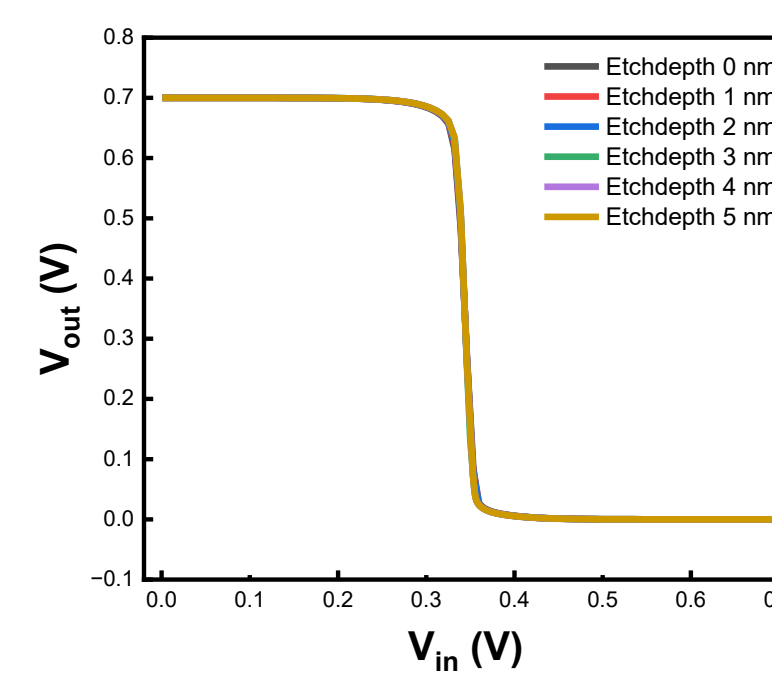


Fig. 5. VTC curve

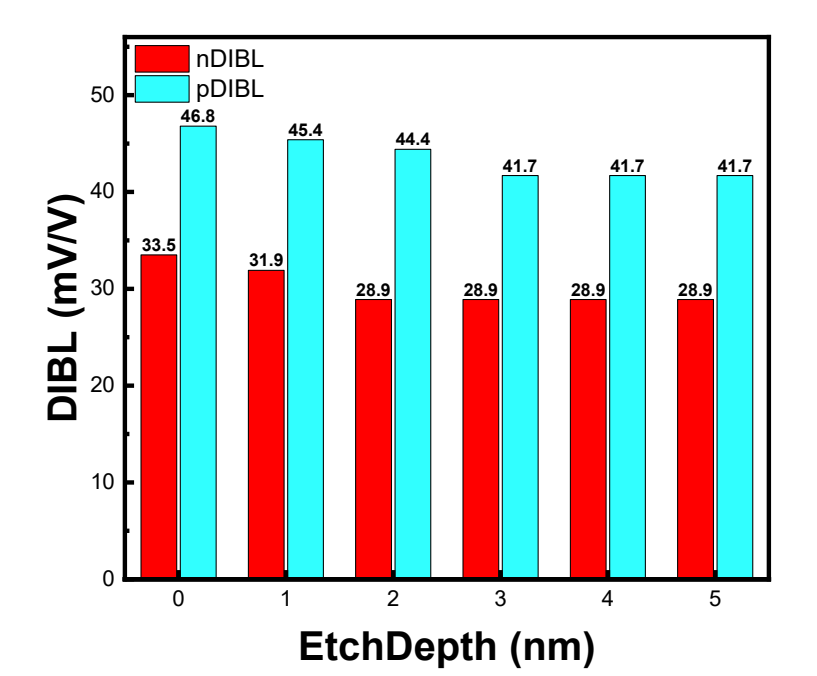


Fig. 6. DIBL in different etch depths

Enhanced gate control minimizes DIBL and steepens subthreshold swing (SS), governed by $SS = \frac{kT}{q} \ln(10) \left(1 + \frac{C_{dep}}{C_{gg}}\right)$. Per $I_{sub} \propto 10^{\frac{V_{gs}-V_{th}}{SS}}$, a smaller SS exponentially accelerates device turn-off. This narrows the N/PMOS conduction overlap, shrinking the short-circuit current skirt to lower dynamic power. However, deeper etching elevates parasitic capacitance (C_{gg}). Based on $f_t = \frac{g_m}{2\pi C_{gg}}$ and $\tau = R_{eff} C_{gg}$, the surging C_{gg} degrades AC response and prolongs delay time, highlighting a critical power-delay trade-off.

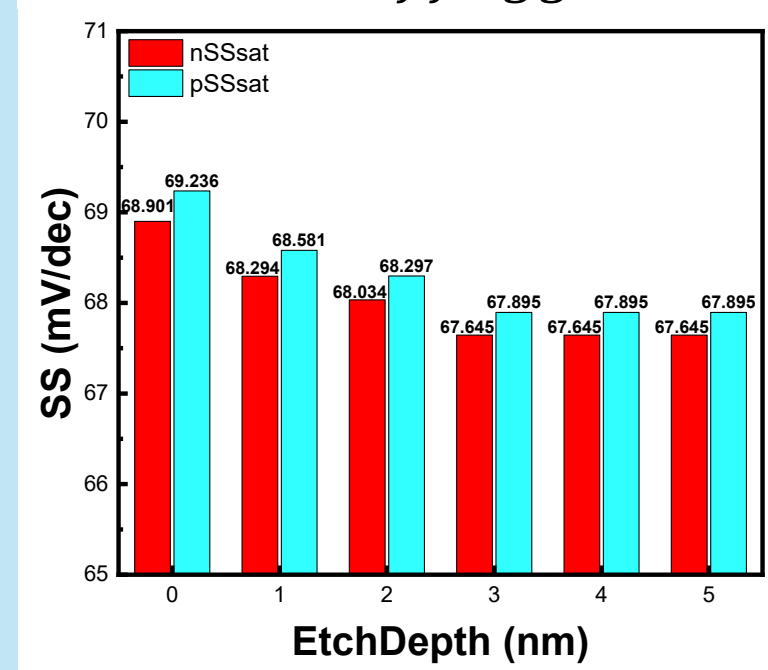


Fig. 7. SS of Outer Wall Forksheet in different etch depths

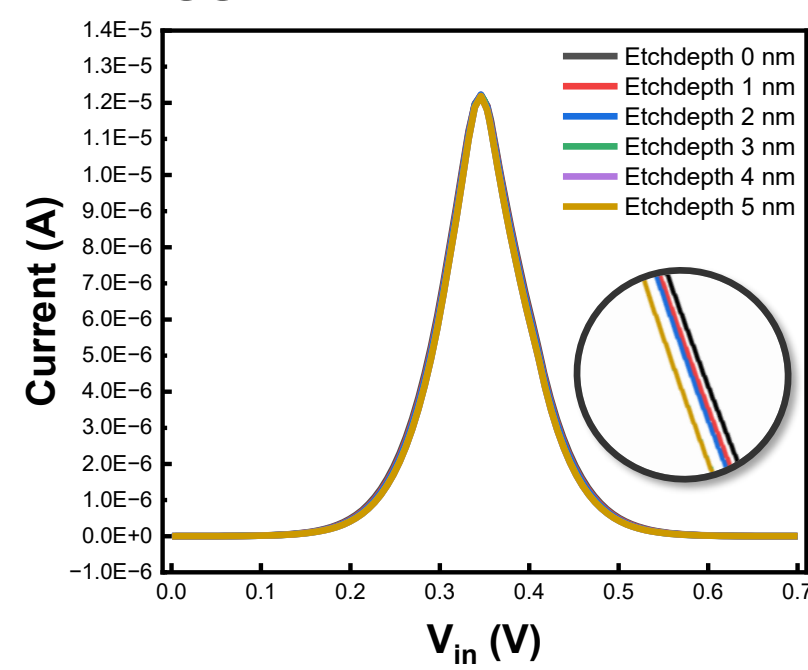
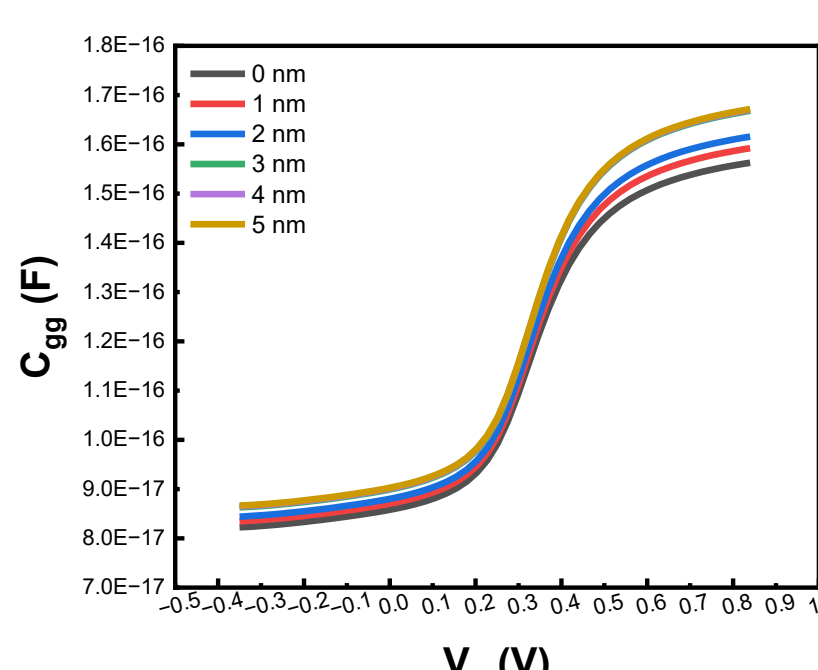
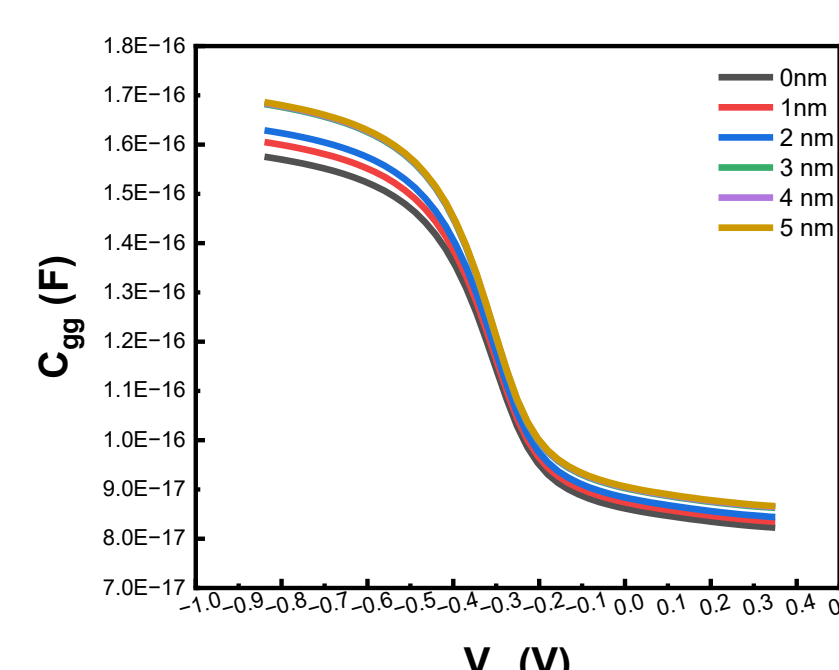


Fig. 8. Short-circuit current versus V_{in}



(a)



(b)

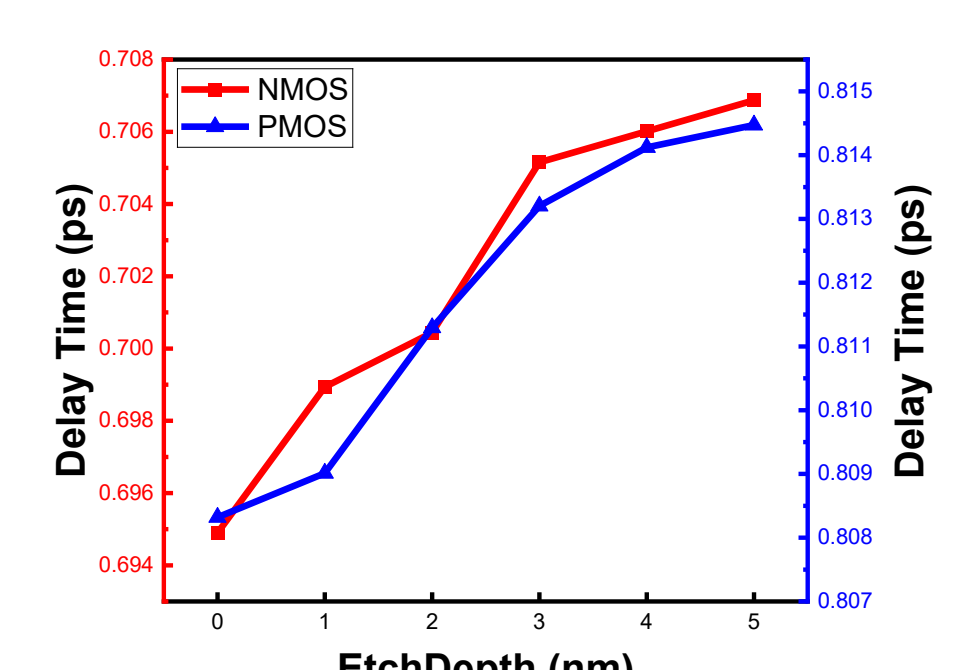


Fig. 10. RC delay time

Conclusion

Outer wall engineering introduces a fundamental power-delay trade-off in sub-3nm Forksheet FETs. While transforming into an Ω -gate effectively minimizes dynamic power and preserves static stability, the severe AC penalty induced by parasitic fringing capacitance cannot be ignored. Ultimately, pinpointing the optimal etch depth is imperative to harvest DC electrostatic benefits without sacrificing high-frequency switching speed in future logic architectures.