

Investigation of Performance Optimization and Electrical Characteristics in Pi-Gate Nanosheet FETs



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Abstract

This study investigates the electrical characteristics of Pi-Gate Nanosheet FETs (NSFETs) using Sentaurus TCAD. A novel gate-extension scheme is analyzed, where extending the gate electrode into the substrate region enhances electrostatic control. Simulation results demonstrate that increasing the gate extension depth (D_{ext}) significantly suppresses off-state leakage current (I_{off}) by three orders of magnitude and improves the subthreshold swing (SS). Furthermore, the total gate capacitance (C_g) is characterized and demonstrated to address the inevitable AC trade-off against DC performance, providing key insights for next-generation transistor designs.

Device Structure

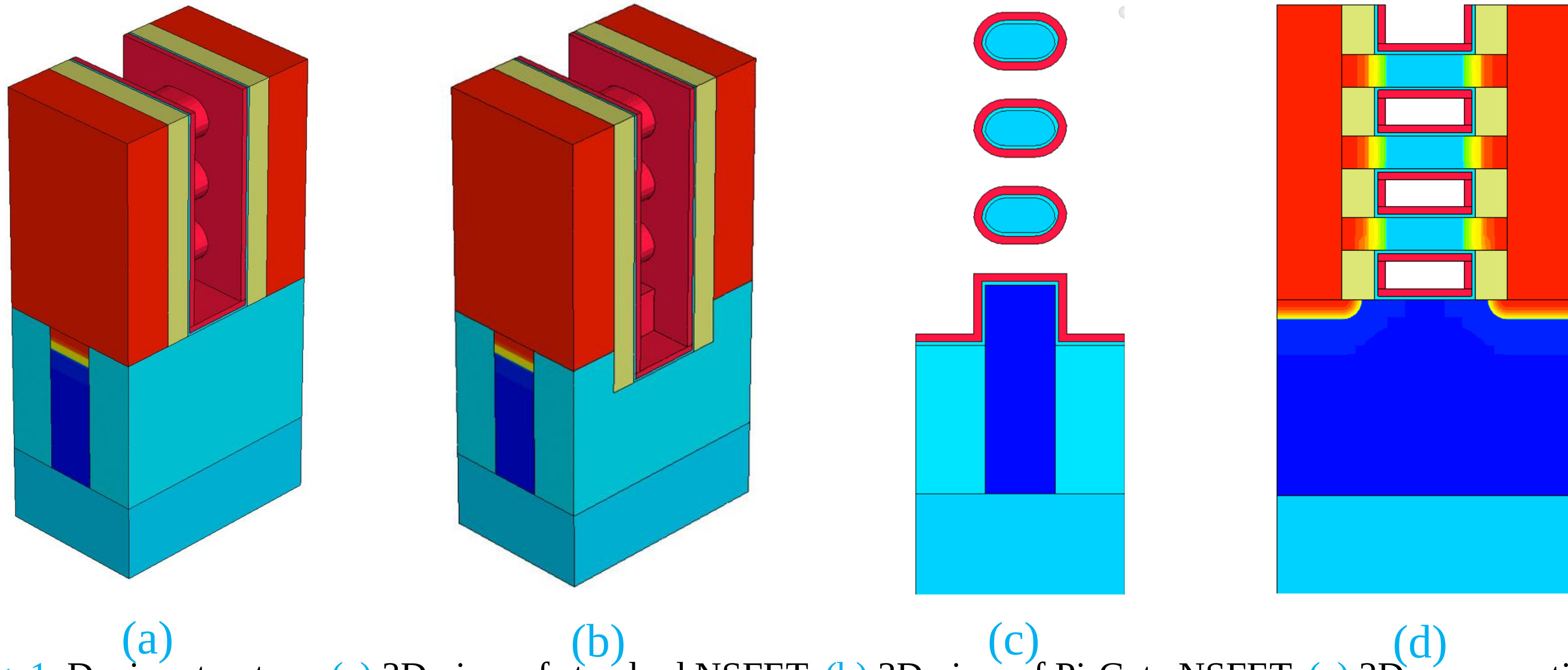


Fig. 1. Device structure. (a) 3D view of standard NSFET, (b) 3D view of Pi-Gate NSFET, (c) 2D cross-section along the gate width direction, (d) 2D cross-section along the channel length direction.

Device Parameter

Device Parameter	Pi-gate	NSFET
Number of Sheets(N_{sheet})	3	3
Gate Length(L_G)	12 nm	12 nm
Gate Extension Depth(D_{ext})	1~10 nm	0 nm
Nanosheet Thickness(T_{sheet})	5 nm	5 nm
Nanosheet Width(W_N)	10 nm	10 nm
Effective Width(W_{eff})	$100 + 2 * D_{ext}$ nm	100 nm
Source/Drain Doping	$1e20 \text{ cm}^{-3}$	$1e20 \text{ cm}^{-3}$
Channel Doping	$1e15 \text{ cm}^{-3}$	$1e15 \text{ cm}^{-3}$
Substrate Doping	$1e15 \text{ cm}^{-3}$	$1e15 \text{ cm}^{-3}$
Active Doping	$1e17 \text{ cm}^{-3}$	$1e17 \text{ cm}^{-3}$
Work Function	4.55 eV	4.55 eV

Fig. 2. Device dimensions and simulation parameters for the standard NSFET and Pi-Gate NSFET.

Simulation Result

The simulation results demonstrate a significant improvement in off-state characteristics as the gate extension depth (D_{ext}) increases. Compared to the standard NSFET ($D_{ext} = 0$), the Pi-Gate structure enhances electrostatic control over the parasitic channel region. The **off-state leakage current (I_{off}) is suppressed by approximately three orders of magnitude** (from $\sim 10^{-9}$ A to $\sim 10^{-12}$ A), accompanied by a **consistent reduction in subthreshold swing (SS)**. Crucially, the **threshold voltage (V_{th}) remains virtually unchanged, indicating no device degradation in this aspect**, while the **on-state current (I_{on}) is successfully maintained** with negligible degradation, indicating that the innovative gate extension improves short-channel effects (SCEs) without sacrificing the high-current drive capability.

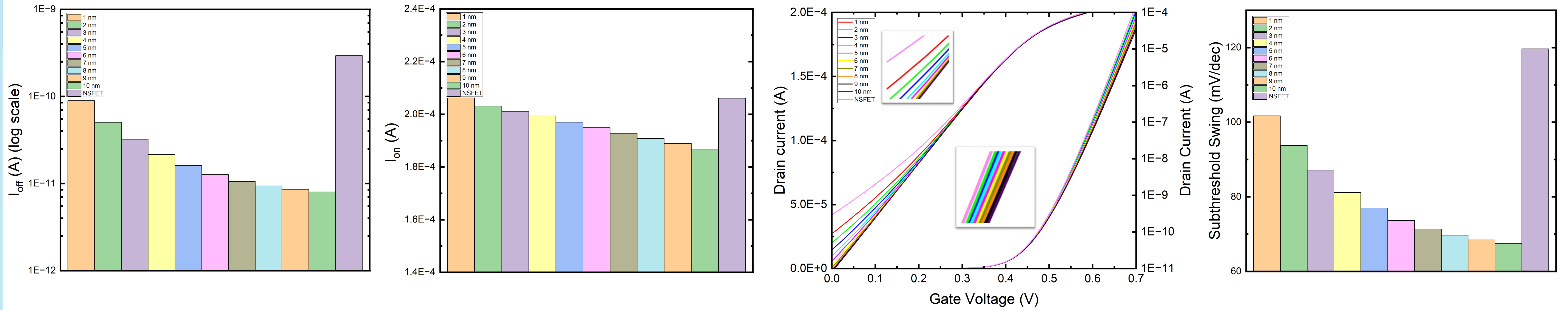


Fig. 3. DC performance comparisons of simulated devices with varying gate extension depths (D_{ext}). (a) Off-state leakage current (I_{off}), (b) On-state drive current (I_{on}), (c) I_d - V_g transfer characteristics, (d) Subthreshold swing (SS).

The 2D current density profiles show that increasing the gate extension depth (D_{ext}) successfully suppresses the parasitic channel leakage path from a high-current zone into a low-current state. The corresponding 1D conduction band (E_C) profile, extracted slightly below the source/drain junctions, confirms that the enhanced gate field effectively lifts the potential barrier, blocking carrier injection through the substrate.

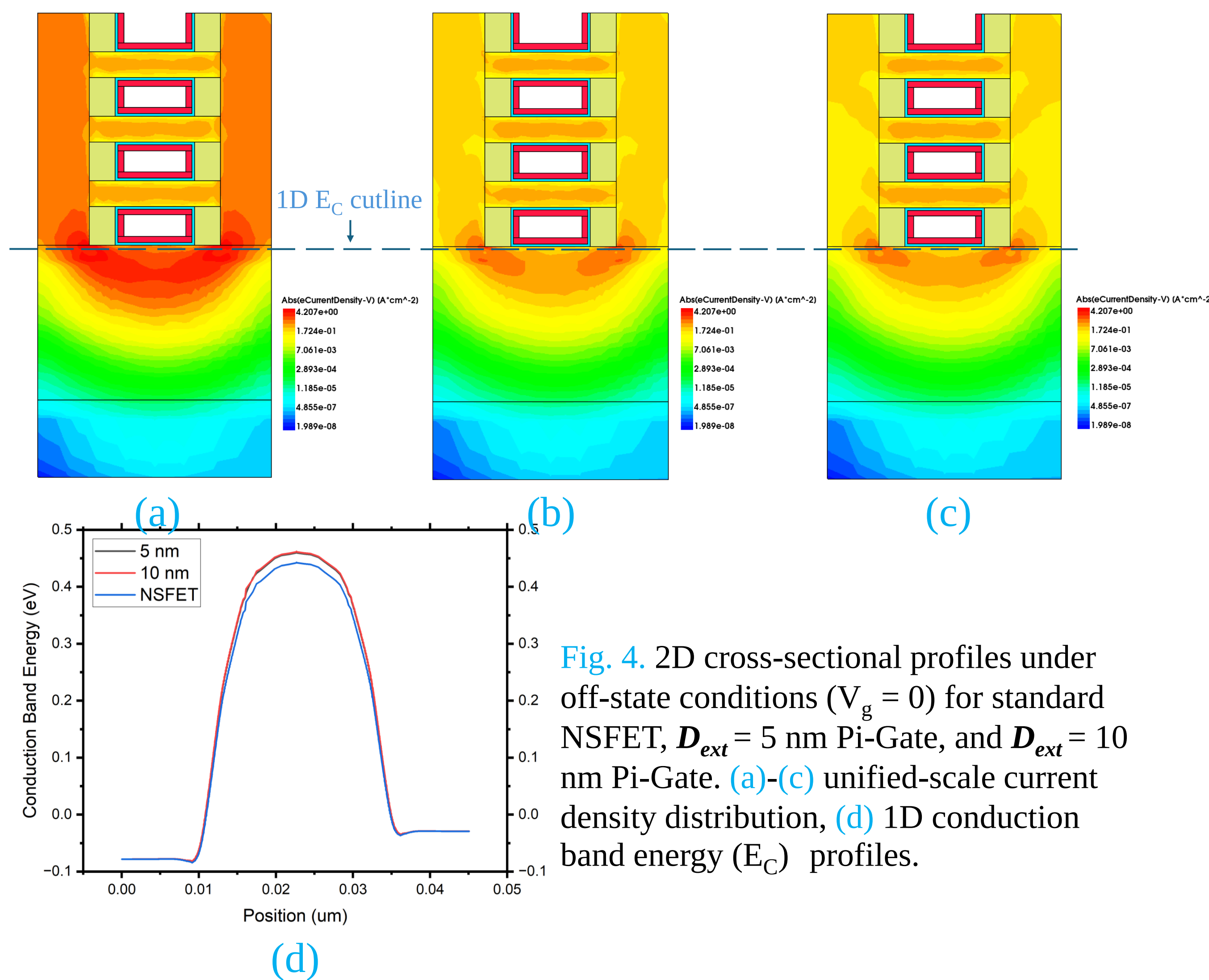


Fig. 4. 2D cross-sectional profiles under off-state conditions ($V_g = 0$) for standard NSFET, $D_{ext} = 5$ nm Pi-Gate, and $D_{ext} = 10$ nm Pi-Gate. (a)-(c) unified-scale current density distribution, (d) 1D conduction band energy (E_C) profiles.

In the strong inversion region ($V_g > 0.4$ V), Total gate capacitance (C_{gg}) increases monotonically with deeper gate extension (D_{ext}).

According to the formula: $C_{gg} \approx \frac{\epsilon_{ox} \times A_{eff}}{T_{ox}}$.

This growth is directly driven by the expanded effective gate area (A_{eff}) overlapping the substrate.

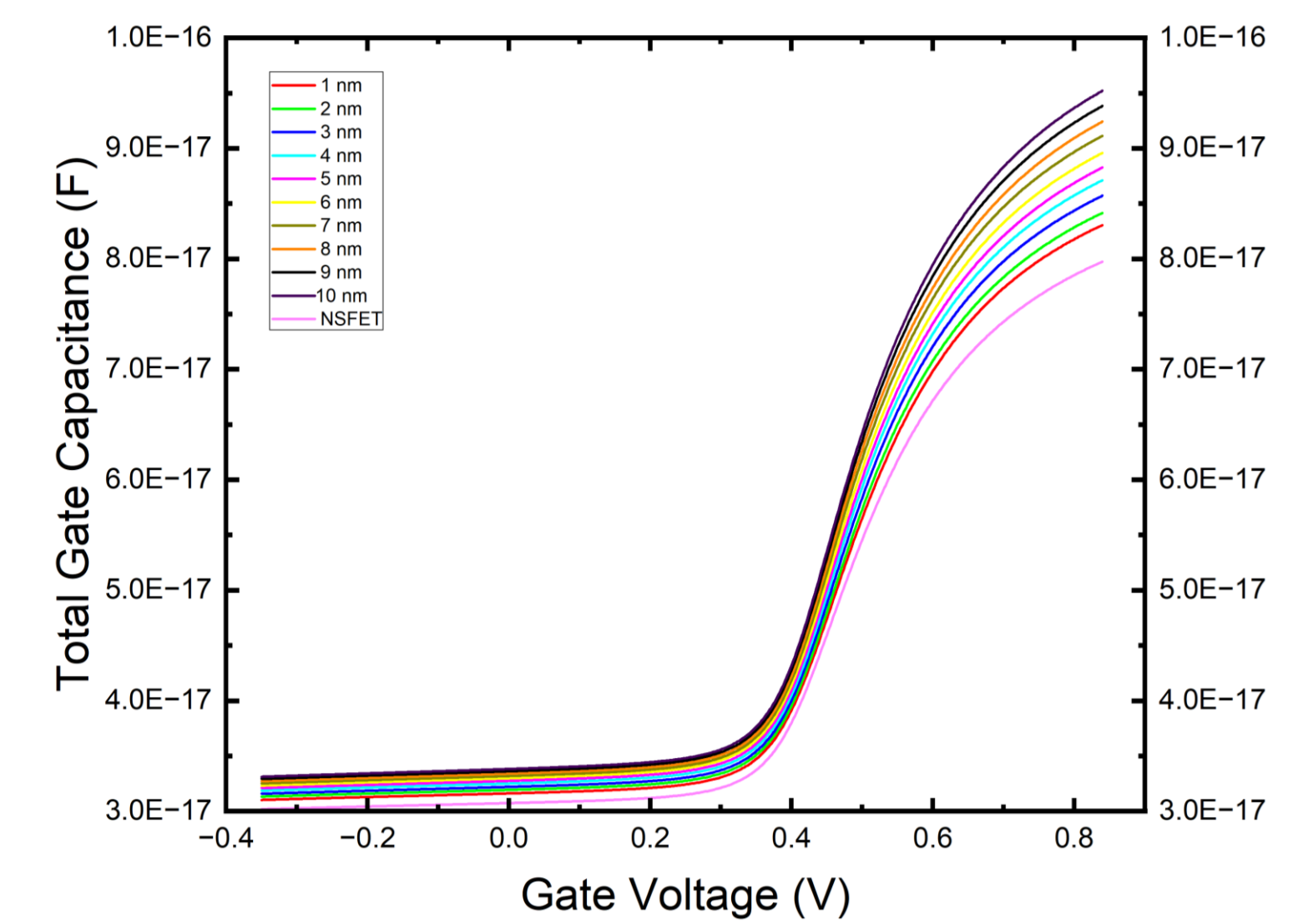


Fig. 5. Total gate capacitance (C_{gg}) as a function of gate voltage (V_g) for simulated devices with various gate extension depths (D_{ext}).

Conclusion

In conclusion, the Pi-Gate architecture provides superior electrostatic control by modulating the substrate region. The enhanced gate electric field successfully lifts the conduction band energy to establish a substantial potential barrier, efficiently blocking carrier injection through the parasitic channel and suppressing the leakage paths into a low-current state. However, the AC characteristics reveal an inherent trade-off: the total gate capacitance exhibits a monotonic increase in the strong inversion region due to the expanded effective gate area overlapping the substrate. This unavoidable parasitic capacitance increment highlights critical design considerations for high-speed switching applications.