

Leakage and Thermal Analysis of NSFETs with Different Substrate Isolation Strategies



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Abstract

We analyze Gate-Induced Drain Leakage(GIDL) and Self-Heating Effects(SHE) in 12nm NSFETs using Sentaurus TCAD. The S-PTS structure effectively suppresses leakage by optimizing electric fields and BTBT. It reduces the maximum temperature to 415.9 K, limiting current degradation to 16.3%. Thus, S-PTS provides the optimal trade-off for advanced 5.9 K and device reliability.

Device Structure

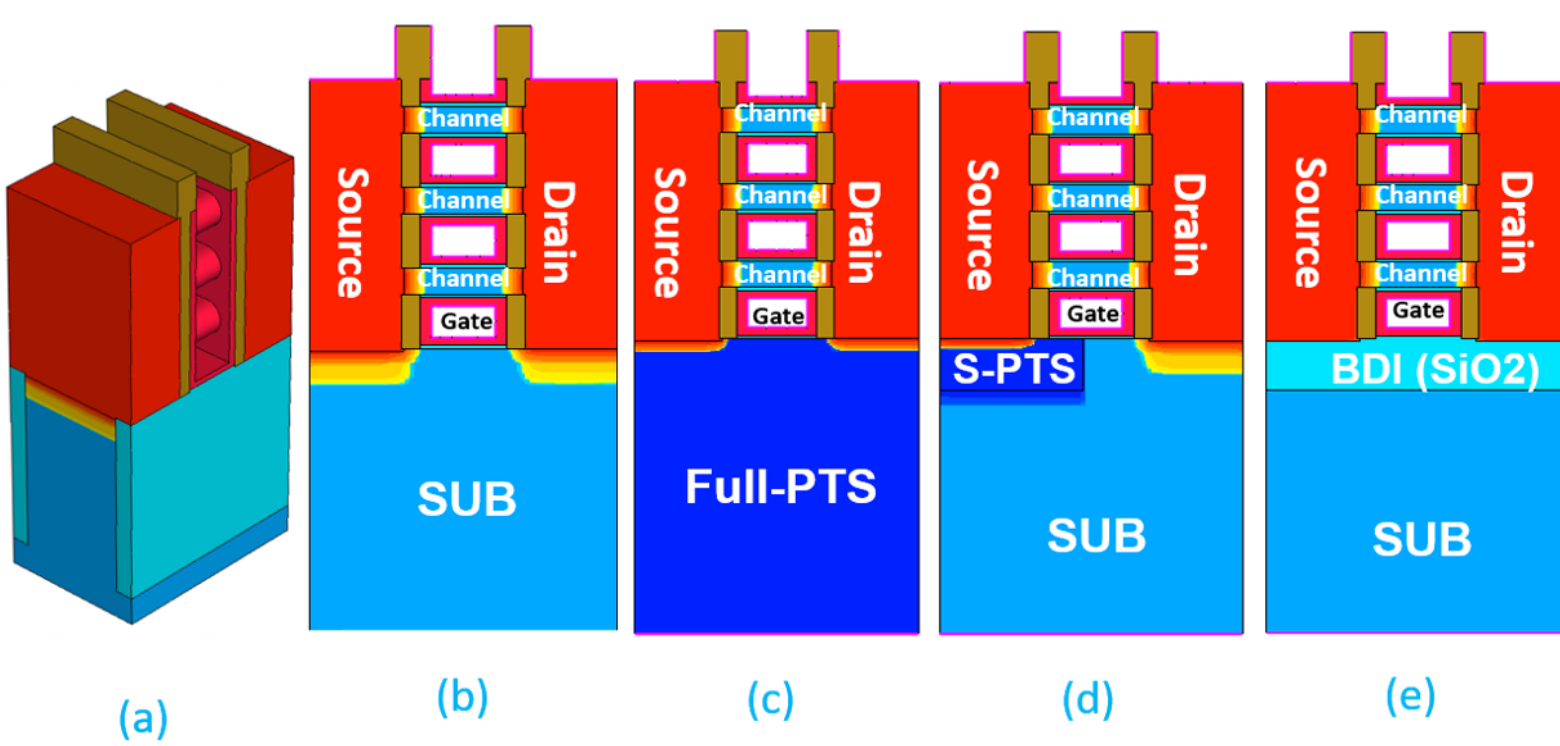


Fig. 1. Device structure. (a) 3D structure, (b) Regular Bulk, (c) Full-PTS, (d) S-PTS, (e) BDI

Parameters	Values
L_G [nm]	12
L_{SD} [nm]	17
L_{SP} [nm]	3.5
T_{CH} [nm]	6
T_{SUS} [nm]	6
T_{HK} [nm]	1.5
T_{Oxide} [nm]	0.6
Width [nm]	30
Channel Doping [cm^{-3}]	10^{17}
S/D Doping [cm^{-3}]	10^{20}
SUB Doping [cm^{-3}]	10^{17}
Full-PTS Doping [cm^{-3}]	5×10^{18}
S-PTS Doping [cm^{-3}]	5×10^{18}

Process Flow

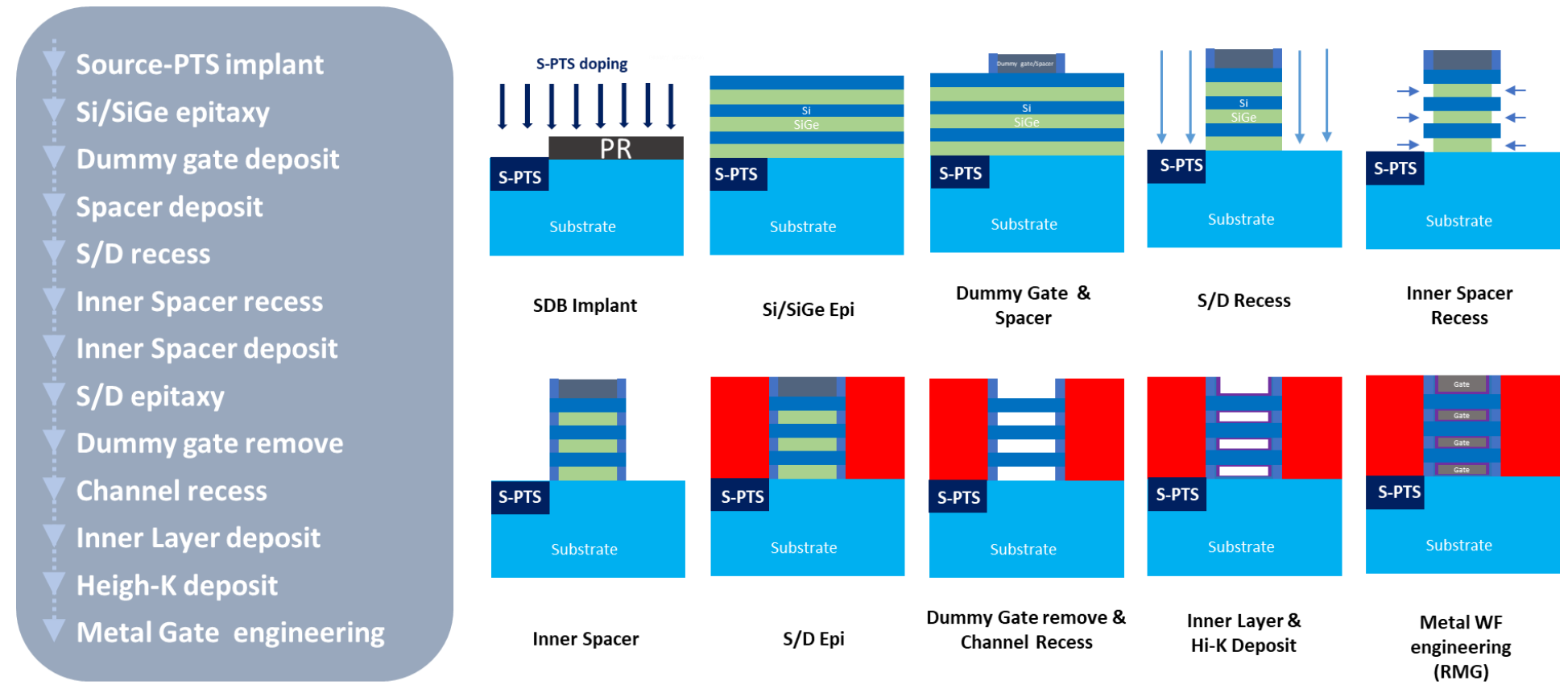


Fig. 2. Process flow of SDB-NSFET.

Simulation Result

Based on Fig.3: It can be observed that under a negative gate bias, the leakage currents of S-PTS and Full-PTS structures are significantly lower than the Regular and BDI structures. It demonstrates their superior capability in suppressing GIDL. Fig.4: The cross-sectional profiles visually indicate that the parasitic leakage path in the Regular structure spreads deeply through the substrate. The introduction of the PTS structure successfully blocks this leakage path beneath the sub-fin region.

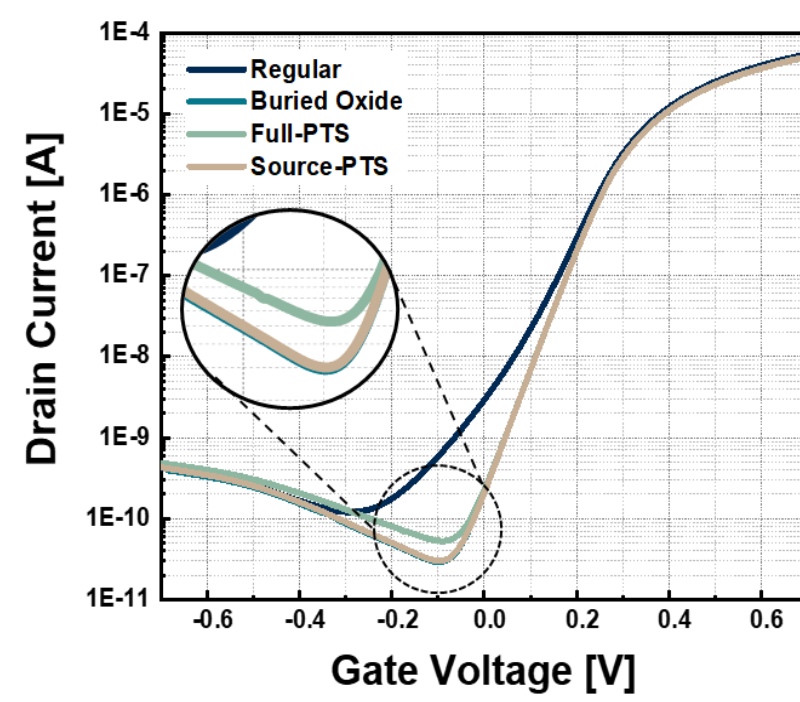


Fig. 3. ID-VG in different structure.

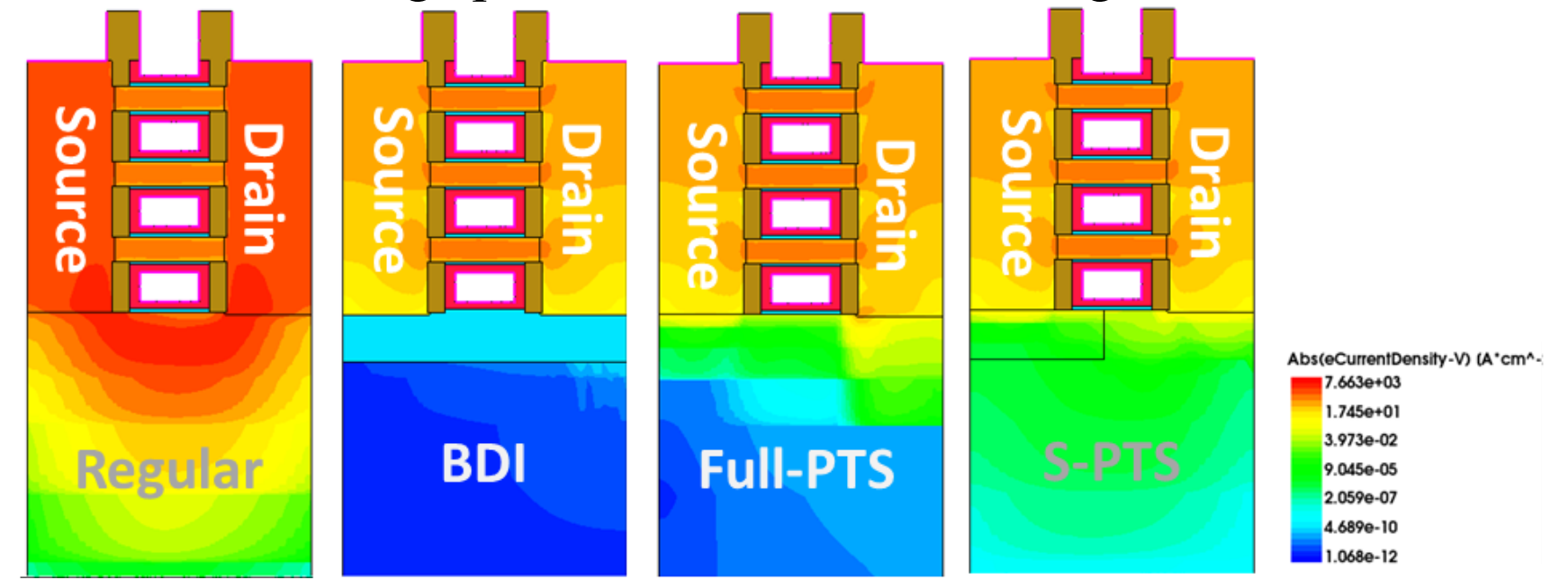


Fig. 4. Electron current density distribution.

The implementation of the isolation scheme directly alters the electrostatic profile at the drain-to-substrate junction. As visually demonstrated in Fig. 6 and Fig. 5, the S-PTS structure effectively relaxes the electric field crowding, significantly lowering the peak electric field at the drain edge compared to the Regular and BDI structures. Subsequently, this optimized electric field directly translates into a suppressed tunneling probability. Driven by the BTBT principle, the weakened electric field in the S-PTS structure minimizes the BTBT generation rate at the drain region, which is corroborated by the 2D generation distribution in Fig. 7. Consequently, the leakage path is blocked at its physical source.

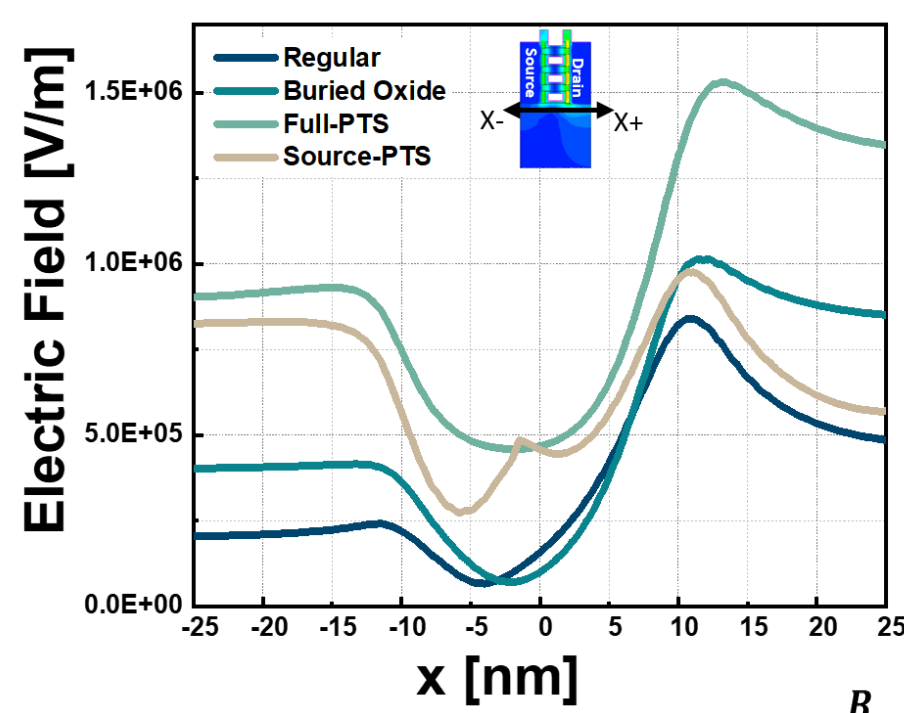


Fig. 5. Electric field. $BTBT \propto E \cdot \exp[-\frac{B}{E}]$

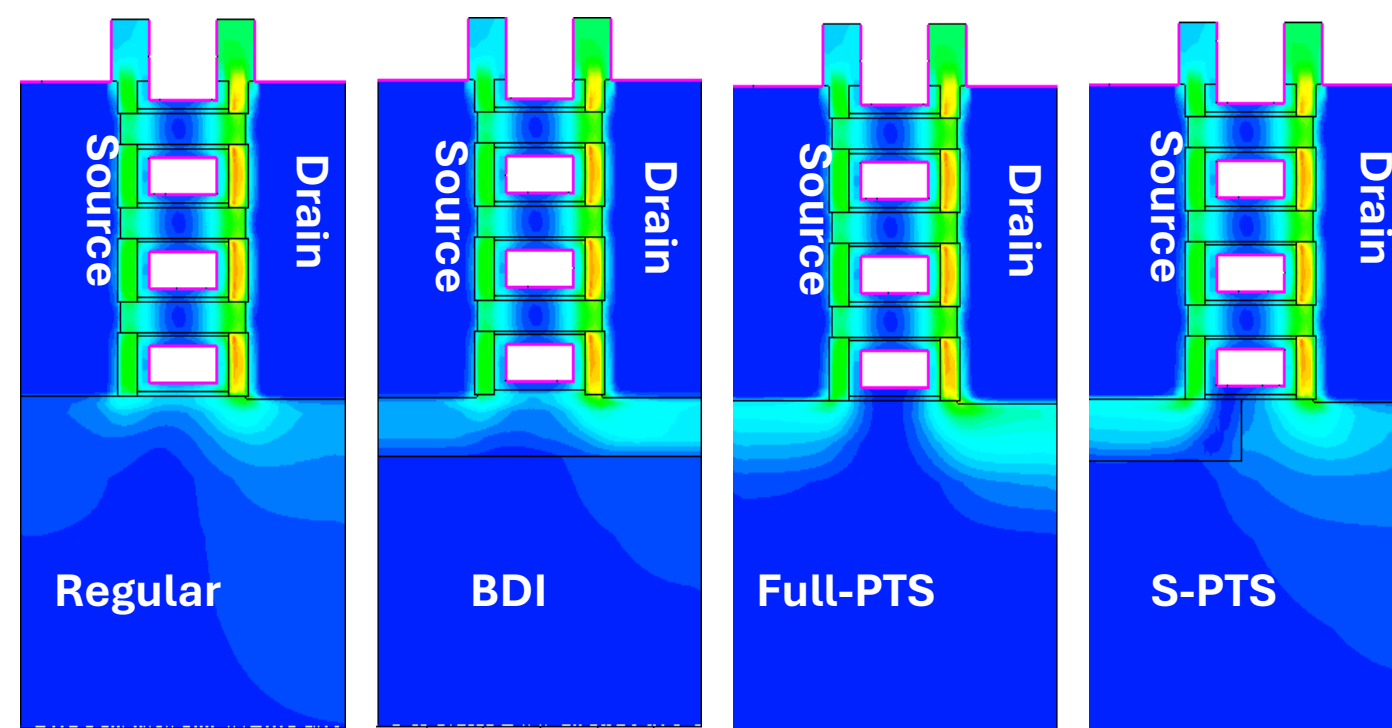


Fig. 6. Electric field distribution.

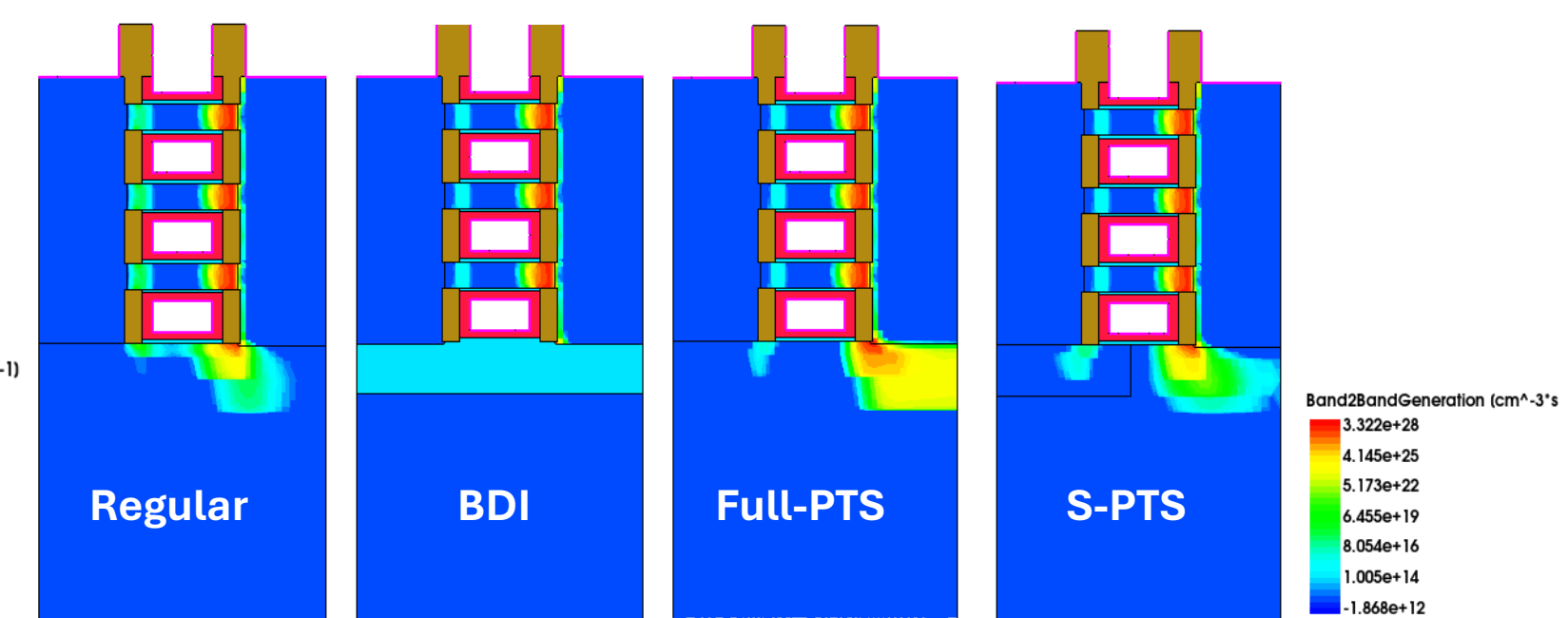


Fig. 7. Band-to-band generation distribution.

From Fig. 8: The heatmaps show that the BDI structure traps heat due to the oxide layer. In contrast, S-PTS provides a more efficient thermal dissipation path, lowering the max temperature to 415.9 K. Based on Fig.9: It illustrates that when self-heating effects are taken into consideration, the on-state drive current of all devices degrades due to a reduction in carrier mobility caused by elevated temperatures. In Fig. 10: Consequently, S-PTS exhibits the highest thermal reliability, limiting the saturation current degradation to only 16.3%. This significantly outperforms the BDI and Regular structures under self-heating conditions.

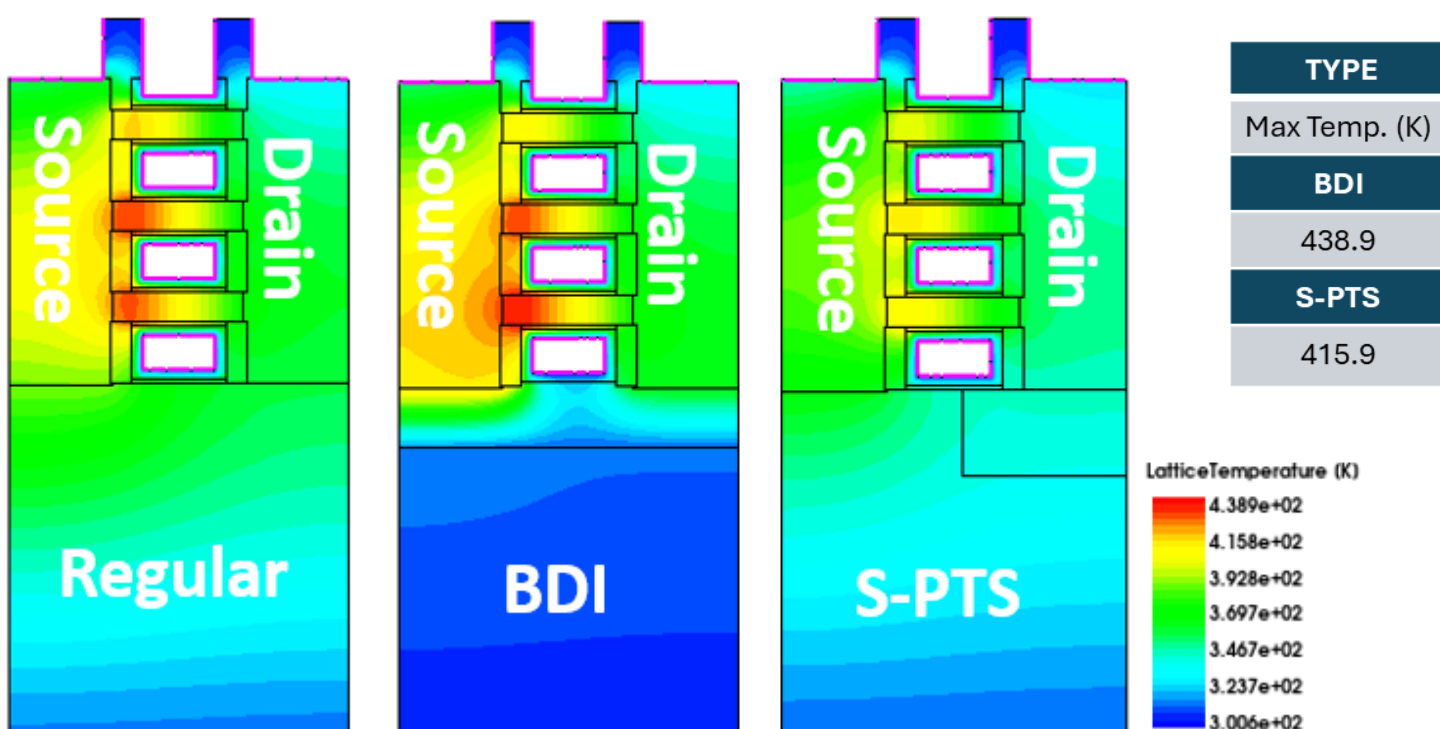


Fig. 8. Lattice temperature distribution.

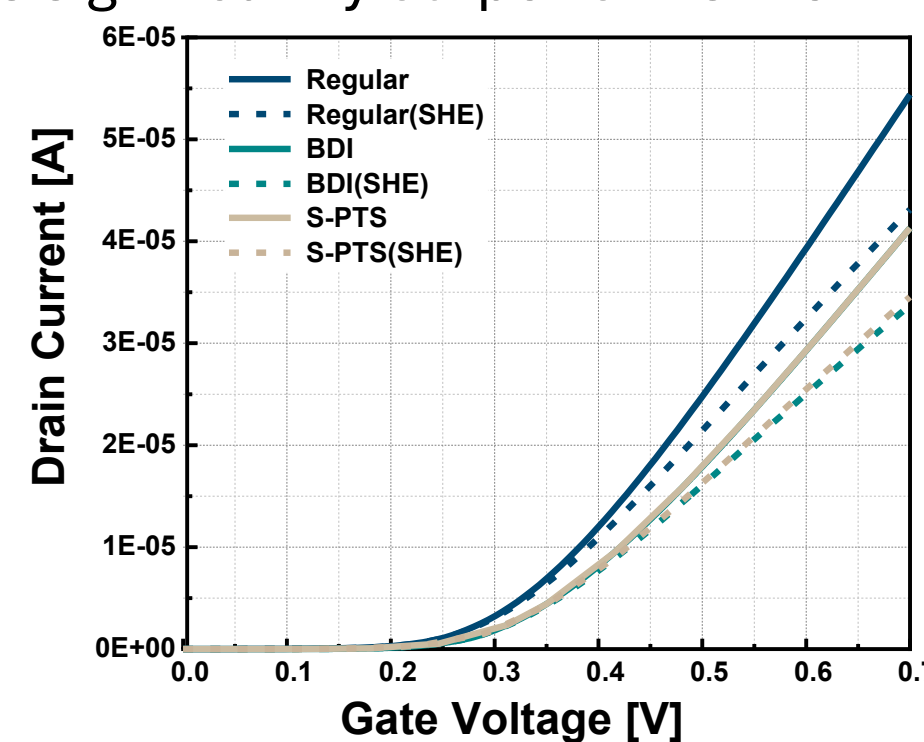


Fig. 9. Curves of various NSFETs considering the SHE.

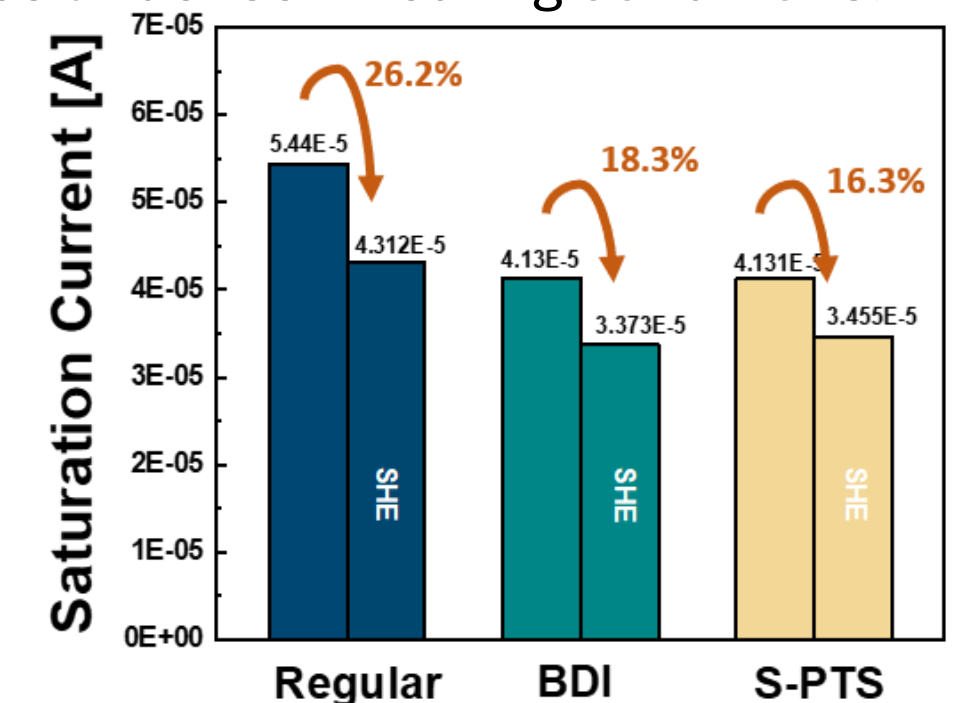


Fig. 10. Impact of SHE on saturation current for Regular, BDI, and S-PTS.

Conclusion

In conclusion, the S-PTS structure provides the optimal trade-off between electrical performance and thermal reliability for 12nm NSFETs. By optimizing the junction electric field, S-PTS effectively suppresses GIDL and BTBT generation, while also lowering the peak lattice temperature to 415.9 K to prevent severe heat trapping. Consequently, it demonstrates minimal saturation current degradation of only 16.3% under self-heating conditions, significantly outperforming both BDI and Regular architectures.